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Learn how to build and use all parts of real-world compilers, including the frontend, optimization pipeline, and a new backend by leveraging the power of LLVM core libraries Key FeaturesGet to grips with effectively using LLVM libraries step-by-step Understand LLVM compiler high-level design and apply the same principles to your own compiler Use compiler-based tools to improve the quality of code in C++ projectsBook Description LLVM was built to bridge the gap between compiler textbooks and actual compiler development. It provides a modular codebase and advanced tools which help developers to build compilers easily. This book provides a practical introduction to LLVM, gradually helping you navigate through complex scenarios with ease when it comes to building and working with compilers. You'll start by configuring, building, and installing LLVM libraries, tools, and external projects. Next, the book will introduce you to LLVM design and how it works in practice during each LLVM compiler stage: frontend, optimizer, and backend. Using a subset of a real programming language as an example, you will then learn how to develop a frontend and generate LLVM IR, hand it over to the optimization pipeline, and generate machine code from it. Later chapters will show you how to extend LLVM with a new pass and how instruction selection in LLVM works. You'll also focus on Just-in-Time compilation issues and the current state of JIT-compilation support that LLVM provides, before finally going on to understand how to develop a new backend for LLVM. By the end of this LLVM book, you will have gained real-world experience in working with the LLVM compiler development framework with the help of hands-on examples and source code snippets. What you will learnConfigure, compile, and install the LLVM frameworkUnderstand how the LLVM source is organizedDiscover what you need to do to use LLVM in your own projectsExplore how a compiler is structured, and implement a tiny compilerGenerate LLVM IR for common source language constructsSet up an optimization pipeline and tailor it for your own needsExtend LLVM with transformation passes and clang toolingAdd new machine instructions and a complete backendWho this book is for This book is for compiler developers, enthusiasts, and engineers who are new to LLVM and are interested in learning about the LLVM framework. It is also useful for C++ software engineers looking to use compiler-based tools for code analysis and improvement, as well as casual users of LLVM libraries who want to gain more knowledge of LLVM essentials. Intermediate-level experience with C++ programming is mandatory to understand the concepts

covered in this book more effectively. The power consumption of microprocessors is one of the most important challenges of high-performance chips and portable devices. In chapters drawn from Piguet's recently published *Low-Power Electronics Design*, this volume addresses the design of low-power microprocessors in deep submicron technologies. It provides a focused reference for specialists involved in systems-on-chips, from low-power microprocessors to DSP cores, reconfigurable processors, memories, ad-hoc networks, and embedded software. *Low-Power Processors and Systems on Chips* is organized into three broad sections for convenient access. The first section examines the design of digital signal processors for embedded applications and techniques for reducing dynamic and static power at the electrical and system levels. The second part describes several aspects of low-power systems on chips, including hardware and embedded software aspects, efficient data storage, networks-on-chips, and applications such as routing strategies in wireless RF sensing and actuating devices. The final section discusses embedded software issues, including details on compilers, retargetable compilers, and coverification tools. Providing detailed examinations contributed by leading experts, *Low-Power Processors and Systems on Chips* supplies authoritative information on how to maintain high performance while lowering power consumption in modern processors and SoCs. It is a must-read for anyone designing modern computers or embedded systems. This is a guidebook for those who want to use computational experiments to support their work in algorithm design and analysis. Numerous case studies and examples show how to apply these concepts. All the necessary concepts in computer architecture and data analysis are covered so that the book can be used by anyone who has taken a course or two in data structures and algorithms.

The Cray Fortran (CFT) compiler is an optimizing compiler. It translates Fortran source statement into object code that makes effective use of the CRAY X-MP and CRAY-1 computer systems. This manual presents techniques that Fortran programmers can employ to optimize the performance of programs compiled under CFT. This new edition has been fully revised and updated to include extensive information on the ARM Cortex-M4 processor, providing a complete up-to-date guide to both Cortex-M3 and Cortex-M4 processors, and which enables migration from various processor architectures to the exciting world of the Cortex-M3 and M4. This book presents the background of the ARM architecture and outlines the features of the processors such as the instruction set, interrupt-handling and also demonstrates how to program and utilize the advanced features available such as the Memory Protection Unit (MPU). Chapters on getting started with IAR, Keil, gcc and CoCoX CoIDE tools help beginners develop program codes. Coverage also includes the important areas of software development such as using the low power features, handling information input/output, mixed language projects with assembly and C, and other advanced topics. Two new chapters on DSP features and CMSIS-DSP software libraries, covering DSP fundamentals and how to write DSP software for the Cortex-M4 processor, including examples of using the CMSIS-DSP library, as well as useful information about the DSP capability of the Cortex-M4 processor A new chapter on the Cortex-M4 floating point unit and how to use it A new chapter on using embedded OS (based on CMSIS-RTOS), as well as details of processor features to support OS operations Various debugging techniques as well as a troubleshooting guide in the appendix topics on software porting from other architectures A full range of easy-to-understand examples, diagrams and quick reference appendices For repairing performance loss or maximizing current potential, this guide aims to provide the information and conceptual framework that will enable readers to be performance experts. Includes information on processor performance, application profiling and hardware considerations.

Android on x86: an Introduction to Optimizing for Intel® Architecture serves two main purposes. First, it makes the case for adapting your applications onto Intel's x86 architecture, including discussions of the business potential, the changing landscape of the Android marketplace, and the unique challenges and opportunities that arise from x86 devices. The fundamental idea is that extending your applications to support x86 or creating new ones is not difficult, but it is imperative to know all of the technicalities. This book is dedicated to providing you with an awareness of these nuances and an understanding of how to tackle them. Second, and most importantly, this book provides a one-stop detailed resource for best practices and procedures associated with the installation issues, hardware optimization issues, software requirements, programming tasks, and performance optimizations that emerge when developers consider the x86 Android devices. Optimization discussions dive into native code, hardware acceleration, and advanced profiling of multimedia applications. The authors have collected this information so that you can use the book as a guide for the specific requirements of each application project. This book is not dedicated solely to code; instead it is filled with the information you need in order to take advantage of x86 architecture. It will guide you through installing the Android SDK for Intel Architecture, help you understand the differences and similarities between processor architectures available in Android devices, teach you to create and port applications, debug existing x86 applications, offer solutions for NDK and C++ optimizations, and introduce the Intel Hardware Accelerated Execution Manager. This book provides the most useful information to help you get the job done quickly while utilizing best practices.

The Definitive Guide to the ARM Cortex-M0 is a guide for users of ARM Cortex-M0 microcontrollers. It presents many examples to make it easy for novice embedded-software developers to use the full 32-bit ARM Cortex-M0 processor. It provides an overview of ARM and ARM processors and discusses the benefits of ARM Cortex-M0 over 8-bit or 16-bit devices in terms of energy efficiency, code density, and ease of use, as well as their features and applications. The book describes the architecture of the Cortex-M0 processor and the programmers model, as well as Cortex-M0 programming and instruction set and how these instructions are used to carry out various operations. Furthermore, it considers how the memory architecture of the Cortex-M0 processor affects software development; Nested Vectored Interrupt Controller (NVIC) and the features it supports, including flexible interrupt management, nested interrupt support, vectored exception entry, and interrupt masking; and Cortex-M0 features that target the embedded operating system. It also explains how to develop simple applications on the Cortex-M0, how to program the Cortex-M0 microcontrollers in assembly and mixed-assembly languages, and how the low-power features of the Cortex-M0 processor are used in programming. Finally, it describes a number of ARM Cortex-M0 products, such as microcontrollers, development boards, starter kits, and development suites. This book will be useful to both new and advanced users of ARM Cortex devices, from students and hobbyists to researchers, professional embedded- software developers, electronic enthusiasts, and even semiconductor product designers. The first and definitive book on the new ARM Cortex-M0 architecture targeting the large 8-bit and 16-bit microcontroller market Explains the Cortex-M0 architecture and how to program it using practical examples Written by an engineer at ARM who was heavily involved in its development Become a better programmer with performance improvement techniques such as concurrency, lock-free programming, atomic operations, parallelism, and memory management Key Features Learn proven techniques from a heavyweight and recognized expert in C++ and high-performance computing Understand the limitations of modern CPUs and their performance impact Find out how you can avoid writing inefficient code and get the best optimizations from the compiler Learn the tradeoffs and costs of writing high-performance programs Book Description The great free lunch of "performance taking care of itself" is over. Until recently, programs got faster by themselves as CPUs were upgraded, but that doesn't happen anymore. The clock frequency of new processors has almost peaked, and while new architectures provide small improvements to existing programs, this only helps slightly. To write efficient software, you now have to know how to program by making good use of the available computing resources, and this book will teach you how to do that. The Art of Efficient Programming covers all the major aspects of writing efficient programs, such as using CPU resources and memory efficiently, avoiding unnecessary computations, measuring performance, and how to put concurrency and multithreading to good use. You'll also learn about compiler optimizations and how to use the programming language (C++) more efficiently. Finally, you'll understand how design decisions impact performance. By the end of this book, you'll not only have enough knowledge of processors and compilers to write efficient programs, but you'll also be able to understand which techniques to use and what to measure while improving performance. At its core, this book is about learning how to learn. What you will learn Discover how to use the hardware computing resources in your programs effectively Understand the relationship between memory order and memory barriers Familiarize yourself with the performance implications of different data structures and organizations Assess the performance impact of concurrent memory accessed and how to minimize it Discover when to use and when not to use lock-free programming techniques Explore different ways to improve the effectiveness of compiler optimizations Design APIs for concurrent data structures and high-performance data structures to avoid inefficiencies Who this book is for This book is for experienced developers and programmers who work on performance-critical projects and want to learn new techniques to improve the performance of their code. Programmers in algorithmic trading, gaming, bioinformatics, computational genomics, or computational fluid dynamics communities will get the most out of the examples in this book, but the techniques are fairly universal. Although this book uses the C++ language, the concepts demonstrated in the book can be easily transferred or applied to other compiled languages such as C, Java, Rust, Go, and more. To the outside world, a "supercomputer" appears to be a single system. In fact, it's a cluster of computers that share a local area network and have the ability to work together on a single problem as a team. Many businesses used to consider supercomputing beyond the reach of their budgets, but new Linux applications have made high-performance clusters more affordable than ever. These days, the promise of low-cost supercomputing is one of the main reasons many businesses choose Linux over other operating systems. This new guide covers everything a newcomer to clustering will need to plan, build, and deploy a high-performance Linux cluster. The book focuses on clustering for high-performance computation, although much of its information also applies to clustering for high-availability (failover and disaster recovery). The book discusses the key tools you'll need to get started, including good practices to use while exploring the tools and growing a system. You'll learn about planning, hardware choices, bulk installation of Linux on multiple systems,

and other basic considerations. Then, you'll learn about software options that can save you hours--or even weeks--of deployment time. Since a wide variety of options exist in each area of clustering software, the author discusses the pros and cons of the major free software projects and chooses those that are most likely to be helpful to new cluster administrators and programmers. A few of the projects introduced in the book include: MPI, the most popular programming library for clusters. This book offers simple but realistic introductory examples along with some pointers for advanced use. OSCAR and Rocks, two comprehensive installation and administrative systems openMosix (a convenient tool for distributing jobs), Linux kernel extensions that migrate processes transparently for load balancing PVFS, one of the parallel filesystems that make clustering I/O easier C3, a set of commands for administering multiple systems Ganglia, OpenPBS, and cloning tools (Kickstart, SIS and G4U) are also covered. The book looks at cluster installation packages (OSCAR & Rocks) and then considers the core packages individually for greater depth or for folks wishing to do a custom installation. Guidelines for debugging, profiling, performance tuning, and managing jobs from multiple users round out this immensely useful book. Building an Optimizing Compiler provides a high-level design for a thorough optimizer, code generator, scheduler, and register allocator for a generic modern RISC processor. In the process it addresses the small issues that have a large impact on the implementation. The book approaches this subject from a practical viewpoint. Theory is introduced where intuitive arguments are insufficient; however, the theory is described in practical terms. Building an Optimizing Compiler provides a complete theory for static single assignment methods and partial redundancy methods for code optimization. It also provides a new generalization of register allocation techniques. A single running example is used throughout the book to illustrate the compilation process. Designed for senior electrical engineering students, this textbook explores the theoretical concepts of digital signal processing and communication systems by presenting laboratory experiments using real-time DSP hardware. This new edition updates the experiments based on the TMS320C6713 (but can easily be adapted to other DSP boards). Each chapter begins with a presentation of the required theory and concludes with instructions for performing experiments to implement the theory. In the process of performing the experiments, students gain experience in working with software tools and equipment commonly used in industry. Over the last ten years, the ARM architecture has become one of the most pervasive architectures in the world, with more than 2 billion ARM-based processors embedded in products ranging from cell phones to automotive braking systems. A world-wide community of ARM developers in semiconductor and product design companies includes software developers, system designers and hardware engineers. To date no book has directly addressed their need to develop the system and software for an ARM-based system. This text fills that gap. This book provides a comprehensive description of the operation of the ARM core from a developer's perspective with a clear emphasis on software. It demonstrates not only how to write efficient ARM software in C and assembly but also how to optimize code. Example code throughout the book can be integrated into commercial products or used as templates to enable quick creation of productive software. The book covers both the ARM and Thumb instruction sets, covers Intel's XScale Processors, outlines distinctions among the versions of the ARM architecture, demonstrates how to implement DSP algorithms, explains exception and interrupt handling, describes the cache technologies that surround the ARM cores as well as the most efficient memory management techniques. A final chapter looks forward to the future of the ARM architecture considering ARMv6, the latest change to the instruction set, which has been designed to improve the DSP and media processing capabilities of the architecture. * No other book describes the ARM core from a system and software perspective. * Author team combines extensive ARM software engineering experience with an in-depth knowledge of ARM developer needs. * Practical, executable code is fully explained in the book and available on the publisher's Website. * Includes a simple embedded operating system. Obtain better system performance, lower energy consumption, and avoid hand-coding arithmetic functions with this concise guide to automated optimization techniques for hardware and software design. High-level compiler optimizations and high-speed architectures for implementing FIR filters are covered, which can improve performance in communications, signal processing, computer graphics, and cryptography. Clearly explained algorithms and illustrative examples throughout make it easy to understand the techniques and write software for their implementation. Background information on the synthesis of arithmetic expressions and computer arithmetic is also included, making the book ideal for newcomers to the subject. This is an invaluable resource for researchers, professionals, and graduate students working in system level design and automation, compilers, and VLSI CAD. Performance tuning is becoming more important than it has been for the last 40 years. Read this book to understand your application's performance that runs on a modern CPU and learn how you can improve it. The 170+ page guide combines the knowledge of many optimization experts from different industries. This book constitutes the proceedings of the 21st International Conference on Verification, Model Checking, and Abstract Interpretation, VMCAI 2020. The 21 papers presented in this volume were carefully reviewed from 44 submissions. VMCAI provides a forum for researchers from the communities of verification, model checking, and abstract interpretation, facilitating interaction, cross-fertilization, and advancement of hybrid methods that combine these and related areas. This guide provides a comprehensive overview of High Performance Computing (HPC) to equip students with a full skill set including cluster setup, network selection, and a background of supercomputing competitions. It covers the system, architecture, evaluating approaches, and other practical supercomputing techniques. As the world's largest supercomputing hackathon, the ASC Student Supercomputer Challenge has attracted a growing number of new talent to supercomputing and has greatly promoted communications in the global HPC community. Enclosed in this book, readers will also find how to analyze and optimize supercomputing systems and applications in real science and engineering cases. FORTRAN has always been intended to be an efficient high-level language, and its adherence to this original design aim has helped it to achieve a dominant position in scientific, engineering and other areas of computing. However, advice on how to obtain the best possible performance has, until now, been scattered through the literature, in brief articles, detailed reports on specific computers, and very general and often superficial chapters in books on FORTRAN programming. **This book, for the first time, deals with the whole topic in a systematic fashion, and every effort has been taken to include only the most up-to-date information, and to present it in a way which clearly distinguishes between the different techniques required for the various types of compiler. **The book begins with an extensive introduction to the subject, including a justification for optimizing, explanations of the hardware of modern computers, and the optimizing techniques used by FORTRAN 77 compilers. The preparatory work required before optimizing begins is covered, followed by a detailed discussion of the procedures which may be applied to source code to achieve the highest efficiency of execution, according to the type of compiler used. IBM and CDC compilers are covered in detail. Program portability is discussed and the use of super-computers introduced. The plans for future FORTRAN are presented. A widely used layout-program appears in an appendix. **FROM THE PREFACE: Throughout its more than two decades of history, one of FORTRAN's main strengths as a programming language has been its adherence to its original design aim of providing efficient program execution. However, advice on how to obtain the best possible performance has hitherto been scattered, being contained either in reports on specific computers and compilers (e.g. Smith et al., 1977), or in parts of various books of rather too general a nature. This book brings together for the first time a detailed survey of the means by which FORTRAN source code may be optimized, and includes other background information which should enable the reader to understand better how a FORTRAN program is processed by a compiler, and subsequently executed. As such, it is intended to help all those who write or run FORTRAN programs to make efficient use of computer resources without making unjustifiably great demands on their own time. **This book should be useful as a reference work for anyone engaged in FORTRAN programming on any scale greater than simple, single-shot, short jobs, and as a supplementary text in any course on FORTRAN programming beyond the preliminary stages. Famed author Jack Ganssle has selected the very best embedded systems design material from the Newnes portfolio. The result is a book covering the gamut of embedded design, from hardware to software to integrated embedded systems, with a strong pragmatic emphasis. Proceedings of the International Conference on Human-centric Computing and Embedded and Multimedia Computing (HumanCom & EMC 2011) will cover topics of HumanCom and EMC, the current hot topics satisfying the world-wide ever-changing needs. Human-centric computing is to create novel solutions so that the humans are always connected, portable, and available. As with pervasive-computing, human-centric computing requires a variety of devices; however, such devices exist simply to obtain inputs from the human and are embedded in objects that humans interact with on a daily basis. Moreover, during the past couple of decades, Information Science technologies influenced and changed every aspect of our lives and our cultures. Without various Information Science technology-based applications, it would be difficult to keep information stored securely, to process information efficiently, and to communicate conveniently. Embedded computing ranges from portable devices such as digital watches and MP3 players, to large stationary installations like traffic lights, factory controllers, or the systems controlling nuclear power plants. Complexity varies from low, with a single microcontroller chip, to very high with multiple units, peripherals and networks mounted inside a large chassis or enclosure. Multimedia computing covers multimedia I/O devices, OS, storage systems, streaming media middleware, continuous media representations, media coding, media processing, etc., and also includes multimedia communications; real-time protocols, end-to-end streaming media, resource allocation, multicast protocols, and multimedia applications; databases, distributed collaboration, video conferencing, 3D virtual environments. This IBM® Redbooks® publication addresses performance tuning topics to help leverage the virtualization strengths of the POWER® platform to solve clients' system resource utilization challenges, and maximize system throughput and capacity. We examine the performance monitoring tools, utilities, documentation, and other resources available to help technical teams provide optimized business

solutions and support for applications running on IBM POWER systems' virtualized environments. The book offers application performance examples deployed on IBM Power Systems™ utilizing performance monitoring tools to leverage the comprehensive set of POWER virtualization features: Logical Partitions (LPARs), micro-partitioning, active memory sharing, workload partitions, and more. We provide a well-defined and documented performance tuning model in a POWER system virtualized environment to help you plan a foundation for scaling, capacity, and optimization. This book targets technical professionals (technical consultants, technical support staff, IT Architects, and IT Specialists) responsible for providing solutions and support on IBM POWER systems, including performance tuning. Coding and testing are often considered separate areas of expertise. In this comprehensive guide, author and Java expert Scott Oaks takes the approach that anyone who works with Java should be equally adept at understanding how code behaves in the JVM, as well as the tunings likely to help its performance. You'll gain in-depth knowledge of Java application performance, using the Java Virtual Machine (JVM) and the Java platform, including the language and API. Developers and performance engineers alike will learn a variety of features, tools, and processes for improving the way Java 7 and 8 applications perform. Apply four principles for obtaining the best results from performance testing Use JDK tools to collect data on how a Java application is performing Understand the advantages and disadvantages of using a JIT compiler Tune JVM garbage collectors to affect programs as little as possible Use techniques to manage heap memory and JVM native memory Maximize Java threading and synchronization performance features Tackle performance issues in Java EE and Java SE APIs Improve Java-driven database application performance This book introduces embedded systems to C and C++ programmers. Topics include testing memory devices, writing and erasing flash memory, verifying nonvolatile memory contents, controlling on-chip peripherals, device driver design and implementation, and more. The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high-performance chips and portable devices. The study of power-saving design methodologies now must also include subjects such as systems on chips, embedded software, and the future of microelectronics. Low-Power Electronics Design covers all major aspects of low-power design of ICs in deep submicron technologies and addresses emerging topics related to future design. This volume explores, in individual chapters written by expert authors, the many low-power techniques born during the past decade. It also discusses the many different domains and disciplines that impact power consumption, including processors, complex circuits, software, CAD tools, and energy sources and management. The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality. They investigate nanotechnologies, optical circuits, ad hoc networks, e-textiles, as well as human powered sources of energy. Low-Power Electronics Design delivers a complete picture of today's methods for reducing power, and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now. More useful techniques, tips, and tricks for harnessing the power of the new generation of powerful GPUs. Today's embedded devices and sensor networks are becoming more and more sophisticated, requiring more efficient and highly flexible compilers. Engineers are discovering that many of the compilers in use today are ill-suited to meet the demands of more advanced computer architectures. Updated to include the latest techniques, The Compiler Design Handbook, Second Edition offers a unique opportunity for designers and researchers to update their knowledge, refine their skills, and prepare for emerging innovations. The completely revised handbook includes 14 new chapters addressing topics such as worst case execution time estimation, garbage collection, and energy aware compilation. The editors take special care to consider the growing proliferation of embedded devices, as well as the need for efficient techniques to debug faulty code. New contributors provide additional insight to chapters on register allocation, software pipelining, instruction scheduling, and type systems. Written by top researchers and designers from around the world, The Compiler Design Handbook, Second Edition gives designers the opportunity to incorporate and develop innovative techniques for optimization and code generation. A Guide to RISC Microprocessors provides a comprehensive coverage of every major RISC microprocessor family. Independent reviewers with extensive technical backgrounds offer a critical perspective in exploring the strengths and weaknesses of all the different microprocessors on the market. This book is organized into seven sections and comprised of 35 chapters. The discussion begins with an overview of RISC architecture intended to help readers understand the technical details and the significance of the new chips, along with instruction set design and design issues for next-generation processors. The chapters that follow focus on the SPARC architecture, SPARC chips developed by Cypress Semiconductor in collaboration with Sun, and Cypress's introduction of redesigned cache and memory management support chips for the SPARC processor. Other chapters focus on Bipolar Integrated Technology's ECL SPARC implementation, embedded SPARC processors by LSI Logic and Fujitsu, the MIPS processor, Motorola 88000 RISC chip set, Intel 860 and 960 microprocessors, and AMD 29000 RISC microprocessor family. This book is a valuable resource for consumers interested in RISC microprocessors. Digital Visual Fortran is the latest version of a major programming language tool used by scientists and engineers. Written by key technical writers from the Digital Visual Fortran product team, Digital Visual Fortran Programmer's Guide presents in printed form the critical portions of the official programmer's guide, previously only available online. The result is the authoritative book on Digital Visual Fortran's features and how to use them to create effective applications. Digital Visual Fortran is the language of choice for computation-intensive scientific and engineering applications, financial applications, and other programs. Digital recently acquired Fortran technology and rights from Microsoft that allows them to use the Microsoft Developer Studio Integrated Development Environment, which is featured in Microsoft's Visual C++ and Visual Basic. The result is that Digital Visual Fortran is much easier to use and looks and works much like Microsoft's industry-leading programming products for other market segments. The official programmer's guide to Digital Visual Fortran for Version 6.0A Authors are experts from the Digital Visual Fortran product group New Digital Fortran version include Microsoft interface and object technologies Learn and implement the latest Arm Cortex-M microcontroller development concepts such as performance optimization, security, software reuse, machine learning, continuous integration, and cloud-based development from industry experts Key Features Learn how to select the best Cortex-M hardware, software, and tools for your project Understand the use of key software components and how to optimize and develop modern applications Get hands-on experience implementing quality software using example code provided in the book Purchase of the print or Kindle book includes a free eBook in the PDF format Book Description Cortex-M has been around since 2004, so why a new book now? With new microcontrollers based on the Cortex-M55 and Cortex-M85 being introduced this year, Cortex-M continues to expand. New software concepts, such as standardized software reuse, have emerged alongside new topics including security and machine learning. Development methodologies have also significantly advanced, with more embedded development taking place in the cloud and increased levels of automation. Due to these advances, a single engineer can no longer understand an entire project and requires new skills to be successful. This book provides a unique view of how to navigate and apply the latest concepts in microcontroller development. The book is split into two parts. First, you'll be guided through how to select the ideal set of hardware, software, and tools for your specific project. Next, you'll explore how to implement essential topics for modern embedded developers. Throughout the book, there are examples for you to learn by working with real Cortex-M devices with all software available on GitHub. You will gain experience with the small Cortex-M0+, the powerful Cortex-M55, and more Cortex-M processors. By the end of this book, you'll be able to practically apply modern Cortex-M software development concepts. What you will learn Familiarize yourself with heuristics to identify the right components for your Cortex-M project Boot code to efficiently start up a Cortex-M device Optimize algorithms with compilers, middleware, and other means Get to grips with machine learning frameworks and implementation techniques Understand security in the embedded space with solutions like TrustZone and TF-M Explore cloud-based development methodologies to increase efficiency Dive into continuous integration frameworks and best practices Identify future trends that could impact Cortex-M software development Who this book is for This book is for practicing engineers and students working with embedded and IoT systems who want to quickly learn how to develop quality software for Arm Cortex-M processors without reading long technical manuals. If you're looking for a book that explains C or assembly language programming for the purpose of creating a single application or mastering a type of programming such as digital signal processing algorithms, then this book is NOT for you. A basic understanding of embedded hardware and software, along with general C programming skills will assist with understanding the concepts covered in this book. Today's embedded and real-time systems contain a mix of processor types: off-the-shelf microcontrollers, digital signal processors (DSPs), and custom processors. The decreasing cost of DSPs has made these sophisticated chips very attractive for a number of embedded and real-time applications, including automotive, telecommunications, medical imaging, and many others—including even some games and home appliances. However, developing embedded and real-time DSP applications is a complex task influenced by many parameters and issues. DSP Software Development Techniques for Embedded and Real-Time Systems is an introduction to DSP software development for embedded and real-time developers giving details on how to use digital signal processors efficiently in embedded and real-time systems. The book covers software and firmware design principles, from processor architectures and basic theory to the selection of appropriate languages and basic algorithms. The reader will find practical guidelines, diagrammed techniques, tool descriptions, and code templates for developing and optimizing DSP software and firmware. The book also covers integrating and testing DSP systems as well as managing the DSP development effort. Digital signal processors (DSPs) are the future of microchips! Includes practical guidelines, diagrammed techniques, tool descriptions, and code templates to aid in the development and optimization of DSP software and firmware Modern computer architectures designed with high-performance microprocessors

offer tremendous potential gains in performance over previous designs. Yet their very complexity makes it increasingly difficult to produce efficient code and to realize their full potential. This landmark text from two leaders in the field focuses on the pivotal role that compilers can play in addressing this critical issue. The basis for all the methods presented in this book is data dependence, a fundamental compiler analysis tool for optimizing programs on high-performance microprocessors and parallel architectures. It enables compiler designers to write compilers that automatically transform simple, sequential programs into forms that can exploit special features of these modern architectures. The text provides a broad introduction to data dependence, to the many transformation strategies it supports, and to its applications to important optimization problems such as parallelization, compiler memory hierarchy management, and instruction scheduling. The authors demonstrate the importance and wide applicability of dependence-based compiler optimizations and give the compiler writer the basics needed to understand and implement them. They also offer cookbook explanations for transforming applications by hand to computational scientists and engineers who are driven to obtain the best possible performance of their complex applications. The approaches presented are based on research conducted over the past two decades, emphasizing the strategies implemented in research prototypes at Rice University and in several associated commercial systems. Randy Allen and Ken Kennedy have provided an indispensable resource for researchers, practicing professionals, and graduate students engaged in designing and optimizing compilers for modern computer architectures. * Offers a guide to the simple, practical algorithms and approaches that are most effective in real-world, high-performance microprocessor and parallel systems. * Demonstrates each transformation in worked examples. * Examines how two case study compilers implement the theories and practices described in each chapter. * Presents the most complete treatment of memory hierarchy issues of any compiler text. * Illustrates ordering relationships with dependence graphs throughout the book. * Applies the techniques to a variety of languages, including Fortran 77, C, hardware definition languages, Fortran 90, and High Performance Fortran. * Provides extensive references to the most sophisticated algorithms known in research. This IBM® Redbooks® publication provides advice and technical information about optimizing and tuning application code to run on systems that are based on the IBM POWER7® and POWER7+™ processors. This advice is drawn from application optimization efforts across many different types of code that runs under the IBM AIX® and Linux operating systems, focusing on the more pervasive performance opportunities that are identified, and how to capitalize on them. The technical information was developed by a set of domain experts at IBM. The focus of this book is to gather the right technical information, and lay out simple guidance for optimizing code performance on the IBM POWER7 and POWER7+ systems that run the AIX or Linux operating systems. This book contains a large amount of straightforward performance optimization that can be performed with minimal effort and without previous experience or in-depth knowledge. This optimization work can: Improve the performance of the application that is being optimized for the POWER7 system Carry over improvements to systems that are based on related processor chips Improve performance on other platforms The audience of this book is those personnel who are responsible for performing migration and implementation activities on IBM POWER7-based servers, which includes system administrators, system architects, network administrators, information architects, and database administrators (DBAs). * Expanded and revised in light of the GNU Compiler Collection (GCC) 4 release in April 2005, this book offers detailed coverage of GCC's somewhat daunting array of options and features and includes several chapters devoted to its support for languages like C, C++, Java, Objective-C, and Fortran. * Though targeting beginner and intermediate developers, this book goes well beyond basic compiler usage, combining instruction of GCC's advanced features and utilities (authconf, libtool, and gprof) with key coding techniques, such as profiling and optimization to show how to build and manage enterprise-level applications. * This is an enormous market. GCC is the defacto compiler collection for hundreds of thousands of open source projects worldwide, a wide variety of commercial development projects, and is the standard compiler for academic programs. The hands-on guide to high-performance coding and algorithm optimization. This hands-on guide to software optimization introduces state-of-the-art solutions for every key aspect of software performance - both code-based and algorithm-based. Two leading HP software performance experts offer comparative optimization strategies for RISC and for the new Explicitly Parallel Instruction Computing (EPIC) design used in Intel IA-64 processors. Using many practical examples, they offer specific techniques for: Predicting and measuring performance - and identifying your best optimization opportunities Storage optimization: cache, system memory, virtual memory, and I/O Parallel processing: distributed-memory and shared-memory (SMP and ccNUMA) Compilers and loop optimization Enhancing parallelism: compiler directives, threads, and message passing Mathematical libraries and algorithms Whether you're a developer, ISV, or technical researcher, if you need to optimize high-performance software on today's leading processors, one book delivers the advanced techniques and code examples you need: Software Optimization for High Performance Computing. This highly relevant and up-to-the-minute book constitutes the refereed proceedings of the Third International Conference on High Performance Embedded Architectures and Compilers, HiPEAC 2008, held in Göteborg, Sweden, January 27-29, 2008. The 25 revised full papers presented together with 1 invited keynote paper were carefully reviewed and selected from 77 submissions. The papers are organized into topical sections on a number of key subjects in the field. This IBM® Redbooks® publication documents and addresses topics to provide step-by-step customizable application and programming solutions to tune application and workloads to use IBM Power Systems™ hardware architecture. This publication explores, tests, and documents the solution to use the architectural technologies and the software solutions that are available from IBM to help solve challenging technical and business problems. This publication also demonstrates and documents that the combination of IBM high-performance computing (HPC) solutions (hardware and software) delivers significant value to technical computing clients who are in need of cost-effective, highly scalable, and robust solutions. First, the book provides a high-level overview of the HPC solution, including all of the components that makes the HPC cluster: IBM Power System S822LC (8335-GTB), software components, interconnect switches, and the IBM Spectrum™ Scale parallel file system. Then, the publication is divided in three parts: Part 1 focuses on the developers, Part 2 focuses on the administrators, and Part 3 focuses on the evaluators and planners of the solution. The IBM Redbooks publication is targeted toward technical professionals (consultants, technical support staff, IT Architects, and IT Specialists) who are responsible for delivering cost-effective HPC solutions that help uncover insights from vast amounts of client's data so they can optimize business results, product development, and scientific discoveries.

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